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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Laurence B. Boucher et al. Ser. No: 09/692,561  
Filing Date: October 18, 2000 Examiner: Maung, Z.  
Atty. Docket No: ALA-002A GAU: 2152

For: INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD  
FOR ACCELERATED PROTOCOL PROCESSING

October 30, 2002

Assistant Commissioner for Patents  
Washington, D.C. 20231

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Fourth Supplemental Information Disclosure Statement per 37 C.F.R. §1.98

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicants bring the following documents to the Examiner's attention. Included with this letter are ninety-one reference documents and a six-page form PTO-1449 listing those documents.

Citation of these documents shall not be construed as an admission that the documents are prior art with respect to the instant invention, a representation that a search has been made, or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on October 30, 2002.

Date: 10-30-02

Mark Lauer

# FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Filing date: October 18, 2000

Inventors: Laurence B. Boucher et al.

Group Art Unit: 2152

Examiner name: Zarni Maung

Attorney Docket No. ALA-002A

INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING

## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A	4,366,538	12/28/82	Johnson et al.	364	200	
	B	5,056,058	10/08/91	Hirata et al.	709	230	
	C	5,097,442	03/17/92	Ward et al.	365	78	
	D	5,629,933	05/13/97	Delp et al.	370	411	
	E	5,664,114	09/02/97	Krech, Jr. et al.	395	200.64	
	F	5,701,516	12/23/97	Cheng et al.	395	842	
	G	5,771,349	06/23/98	Picazo, Jr. et al.	395	188.01	
	H	5,794,061	08/11/98	Hansen et al.	395	800.01	
	I	5,802,580	09/01/98	McAlpice	711	149	
	J	5,809,328	09/15/98	Nogales et al.	395	825	
	K	5,815,646	09/29/98	Purcell et al.	395	163	

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## Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	L	PCT/US98/24943 (WO 00/13091)	03/09/00	International				
	M	WO 99/65219 (PCT/US99/13184)	12/16/99	International				

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

N	Internet pages entitled "Hardware Assisted Protocol Processing", (which Eugene Feinber is working on), 1 page, printed 11/25/98.
O	Zilog product Brief entitled "Z85C30 CMOS SCC Serial Communication Controller", Zilog Inc., 3 pages, 1997.
P	Internet pages of Xpoint Technologies www.xpoint.com website, 5 pages, printed 12/19/97.
Q	Internet pages entitled: Asante and 100BASE-T Fast Ethernet. 7 pages, printed 5/27/97.

Examiner

Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



U.S. Department of Commerce, Patent and Trademark Office

Application No.: 09/692,561

**FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

Filing date: October 18, 2000

Inventors: Laurence B. Boucher et al.

Group Art Unit: 2152

**INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR  
ACCELERATED PROTOCOL PROCESSING**

Examiner name: Zarni Maung

Attorney Docket No. ALA-002A

## U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A	5,913,028	06/15/99	Wang et al.	395	200.33	10/06/95
	B	5,931,918	8/3/99	Row et al	709	300	
	C	5,935,205	8/10/99	Murayama et al.	709	216	
	D	5,937,169	8/10/99	Connery et al.	395	200.8	
	E	5,941,969	8/24/99	Ram et al.	710	128	
	F	5,941,972	8/24/99	Hoese et al.	710	129	
	G	5,950,203	9/7/99	Stakuis et al.	707	10	
	H	6,005,849	12/21/99	Roach et al.	370	276	
	I	6,009,478	12/28/99	Panner et al.	710	5	
	J	6,016,513	01/18/00	Lowe	709	250	
	K	6,026,452	02/15/00	Pitts	710	56	

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## Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	L	WO 01/05107 A1 (PCT/US00/19006) ✓	01/18/01	International				
	M	WO 01/05116 A2 (PCT/US00/19243) ✓	01/18/01	International				

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	N ✓	Internet pages entitled: A Guide to the Paragon XP/S-A7 Supercomputer at Indiana University. 13 pages, printed 12/21/98.
	O ✓	Richard Stevens, "TCP/IP Illustrated, Volume 1, The Protocols", pages 325-326 (1994).
	P ✓	Internet pages entitled: Northridge/Southbridge vs. Intel Hub Architecture, 4 pages, printed 2/19/01.
	Q ✓	Gigabit Ethernet Technical Brief, Achieving End-to-End Performance. Alteon Networks, Inc., First Edition, September 1996.

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U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/692,561
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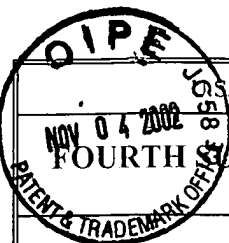
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A	6,044,438	03/28/00	Olnowich	711	130	
	B	6,047,356	04/04/00	Anderson, et al.	711	129	
	C	6,057,863	05/02/00	Olarig	345	520	
	D	6,065,096	05/16/00	Day, et al.	711	114	
	E	6,141,705	10/31/00	Anand, et al.	710	15	<b>RECEIVED</b> <b>NOV 05 2002</b> Technology Center 2100
	F	6,246,683	06/12/01	Connery, et al.	370	392	
	G	5,280,477	01/18/94	Trapp	370	85.1	
	H	5,448,566	09/05/95	Richter et al.	370	94.1	
	I	5,634,127	05/27/97	Cloud et al.	395	680	
	J	5,751,715	05/12/98	Chan et al.	370	455	
	K	5,878,225	03/02/99	Bilansky et al.	395	200.57	

Foreign Patent Documents								
							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	L	WO 01/05123 A1 (PCT/US00/18976)	01/18/01	International				
	M	WO 01/40960A1 (PCT/US00/32660)	06/07/01	International				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
N	Internet pages directed to Technical Brief on Alteon Ethernet Gigabit NIC technology, www.alteon.com, 14 pages, printed 3/15/97.
O	VIA Technologies, Inc. article entitled "VT8501 Apollo MVP4", pages i-iv, 1-11, cover and copyright page, revision 1.3, Feb. 1, 2000.
P	iReady News Archives article entitled "iReady Rounding Out Management Team with Two Key Executives", <a href="http://www.ireadyco.com/archives/keyexec.html">http://www.ireadyco.com/archives/keyexec.html</a> , 2 pages, printed 11/28/98.
Q	"Toshiba Delivers First Chips to Make Consumer Devices Internet-Ready Based On iReady's Design," Press Release October, 1998, 3 pages, printed 11/28/98.

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U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A	5,996,024	11/30/99	Blumenau	709	301	
	B	6,173,333	01/09/01	Jolitz et al.	709	240	
	C	2001/0025315A1		Jolitz			01/10/01
	D	2001/0004354A1		Jolitz			01/10/01
	E	5,058,110	10/15/91	Beach et al.	370	85.6	
	F	6,021,446	02/01/00	Gentry et al.	709	303	
	G	6,356,951	03/12/02	Gentry et al.	709	250	
	H	6,389,468	05/14/02	Muller et al.	709	226	
	I	6,434,651	08/13/02	Gentry, Jr.	710	260	
	J	6,427,169	07/30/02	Elzur	709	224	
	K	6,449,656	09/10/02	Elzur et al.	709	236	
	L	6,453,360	09/17/02	Muller et al.	709	250	

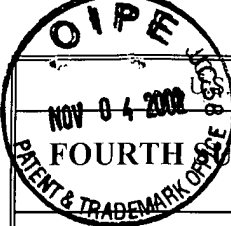
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Foreign Patent Documents							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	G	WO 01/04770 A2 (PCT/US00/18939)	01/18/01	International				
	H							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
I	Internet pages from iReady Products, web site <a href="http://www.ireadyco.com/products.html">http://www.ireadyco.com/products.html</a> , 2 pages, downloaded 11/25/98.
J	iReady News Archives, Toshiba, iReady shipping Internet chip, 1 page, printed 11/25/98.
K	Interprophet article entitled "Technology", <a href="http://www.interprophet.com/technology.html">http://www.interprophet.com/technology.html</a> , 17 pages, printed 3/1/00.
L	iReady Corporation, article entitled "The I-1000 Internet Tuner", 2 pages, date unknown.

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	Attorney Docket No. ALA-002A

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

A	iReady article entitled "About Us Introduction", Internet pages from <a href="http://www.iReadyco.com/about.html">http://www.iReadyco.com/about.html</a> , 3 pages, printed 11/25/98.
B	iReady News Archive article entitled "Revolutionary Approach to Consumer Electronics Internet Connectivity Funded", San Jose, CA, November 20, 1997. 2 pages, printed 11/2/98.
C	iReady News Archive article entitled "Seiko Instruments Inc. (SII) INTRODUCES WORLD'S FIRST INTERNET-READY INTELLIGENT LCD MODULES BASED ON IREADY TECHNOLOGY," Santa Clara, CA and Chiba, Japan, October 26, 1998. 2 pages, printed 11/2/98.
D	NEWSwatch article entitled "iReady internet Tuner to Web Enable Devices", Tuesday, November 5, 1996, printed 11/2/98.
E	EETimes article entitled "Tuner for Toshiba, Toshiba Taps iReady for Internet Tuner", by David Lammers, 2 pages, printed 11/02/98.
F	"Comparison of Novell Netware and TCP/IP Protocol Architectures", by J.S. Carbone, 19 pages, printed 4/10/98.
G	Adaptec article entitled "AEA-7110C-a DuraSAN product", 11 pages, printed 10/1/01.
H	iSCSI HBA article entitled "iSCSI and 2Gigabit fibre Channel Host Bus Adapters from Emulex, QLogic, Adaptec, JMI", 8 pages, printed 10/01/01.
I	iSCSI HBA article entitled "FCE-3210/6410 32 and 64-bit PCI-to-Fibre Channel HBA", 6 pages, printed 10/01/01.
J	iSCSI HBA article entitled "iSCSI Storage", 6 pages, printed 10/01/01.
K	"Two-Way TCP Traffic Over Rate Controlled Channels: Effects and Analysis", by Kalampoukas et al., IEEE Transactions on Networking, vol. 6, no. 6, December 1998.
L	iReady News article entitled "Toshiba Delivers First Chips to Make Consumer Devices Internet-Ready Based on iReady Design", Santa Clara, CA, and Tokyo, Japan, October 14, 1998, printed 11/2/98.
M	United States Patent Application No. 08/964,304, by Napolitano, et al., entitled "File Array Storage Architecture", filed 11/04/97.
N	"File System Design For An NFS File Server Appliance", Article by D. Hitz, et al., 13 pages.
O	Adaptec Press Release article entitled "Adaptec Announces EtherStorage Technology", 2 pages, May 4, 2000, printed 6/14/00.
P	Adaptec article entitled "EtherStorage Frequently Asked Questions", 5 pages, printed 7/19/00.
Q	Adaptec article entitled "EtherStorage White Paper", 7 pages, printed 7/19/00.

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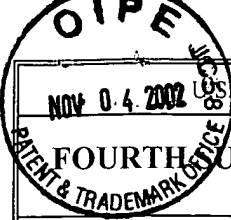
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		Group Art Unit: 2152
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INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING		Attorney Docket No. ALA-002A
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
A	CIBC World Markets article entitled "Computers; Storage", by J. Berlino et al., 9 pages, dated August 7, 2000.	
B	Merrill Lynch article entitled "Storage Futures", by S. Milunovich, 22 pages, dated May 10, 2000.	
C	CBS Market Watch article entitled "Montreal Start-Up Battles Data Storage Bottleneck", by S. Taylor, dated March 5, 2000, 2 pages, printed 3/7/00.	
D	Internet-draft article entitled "SCSI/TCP (SCSI over TCP)", by J. Satran et al., 38 pages, dated February 2000, printed 5/19/00.	
E	Article entitled "LPP: A New Network Subsystem Architecture for Server Systems", by P. Druschel and G. Banga, Rice University, 15 pages.	
F	Internet RFC/STD/FYI/BCP Archives article with heading "RFC2140" entitled "TCP Control Block Interdependence", web address <a href="http://www.faqs.org/rfcs/rfc2140.html">http://www.faqs.org/rfcs/rfc2140.html</a> , 9 pages, printed 9/20/02.	
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